11.7 A Fast-Settling PLL Frequency Synthesizer with Direct Frequency Presetting

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One of the challenges in wireless communication is the development of fast-settling PLL frequency synthesizers with low noise and spurs. The settling speeds of the synthesizers determine how fast a communication channel can be switched from one frequency to another and how fast the system can be turned on or off. In order to realize a fast-settling PLL frequency synthesizer, dynamic loop-bandwidth control has been proposed [1][2]. However, the loop bandwidth is limited by channel spacing and the requirement for low spurs. Recently fractional-N PLL frequency synthesizers were proposed [3][4], but they produce additional fractional spurs that are hard to remove.

This paper proposes a fast-settling PLL synthesizer with a direct frequency-presetting function. In the synthesizer, we developed a mixed-signal voltage controlled oscillator (VCO) whose frequency can be directly and accurately preset by a digital signal depending on the divider ratio N. The frequency-presetting method can greatly reduce the settling time and avoid the tradeoff between settling time and phase noise or spurs. The synthesizer can automatically compensate for the variation of frequency with temperature and operate correctly over a wide range of chip temperatures.

Figure 11.7.1 shows the block diagram of the PLL frequency synthesizer. It consists of six blocks: a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), a mixed-signal VCO, a pulse-swallow divider, and a digital controller. The digital controller not only outputs the divider ratio N but also directly presets the frequency of the VCO with a frequency-presetting digital signal C. The digital signal C presets the output frequency of the VCO with very small initial frequency error. Then the output voltage V_a of the loop filter precisely tunes the frequency of the VCO. Therefore the frequency synthesizer can settle down in a very short time. Using this method, the settling time is not related to the frequency step.

Figure 11.7.2 shows the proposed mixed-signal VCO. The delay cells in the VCO are controlled by three signals: V_c, V_t and V_p. The presetting module outputs the signal V_c that depends on the frequency-presetting digital signal C and the output signal V_a of the loop filter. The signal V_c can preset and tune the oscillation frequency of the VCO. A temperature sensor generates the signal V_t to keep the output frequency constant over temperature. An external signal V_p is used to adjust the center frequency error due to process variation.

Figure 11.7.3 shows the proposed delay cell circuit in the VCO. It is a full-swing differential inverter with parallel active loads. Transistors $M1$ and $M2$ form the feed-forward circuit to speed up the transition between V_{DD} and ground. The signal V_c adjusts the drain currents of $M3$ and $M4$ and controls the delay time to tune the oscillation frequency. Transistors $M5$ and $M6$ are used to compensate the center frequency variation caused by process variations. Transistors $M7$ and $M8$ compensate the frequency variation caused by changes in temperature.

Figure 11.7.4 shows the schematic of the mixed-signal presetting module. When the signal C [6:0] is input to the presetting module, the module outputs the voltage signal V_c to preset the oscillation frequency of the VCO with a small initial frequency error. Then the output signal V_a of the loop filter accurately tunes the oscillation frequency by controlling the current in $M11$. We designed an additional current compensation network to accurately and linearly preset frequency within +/-1MHz. We designed the VCO gain K_v to be much smaller than that of a conventional VCO. Having a small K_v reduces phase noise. Furthermore, a smaller K_v results in smaller capacitance in the loop filter, which saves chip area for a PLL with on-chip capacitors.

The presetting module includes a temperature sensor and compensation circuit. The circuit monitors the chip temperature and outputs the signal V_t to compensate the VCO frequency variation with chip temperature. The other parts of the synthesizer are designed as in a conventional circuit. The loop filter is second order. We set the reference frequency f_r to 1MHz. To maintain the system stability with process and temperature variation, we chose the loop bandwidth to be $f_r/15$, and the phase margin to be 53°. To reduce capacitor area in the loop filter, we used a 100μA charge pump current.

The prototype synthesizer was implemented in a 0.35μm 3.3V CMOS process. Figure 11.7.7 shows the chip micrograph. The loop filter and digital controller are integrated on chip. The whole chip area is 0.4mm^2. The measured output frequency is 560 to 820MHz; the VCO gain is 20 to 25MHz/V; the resolution of the frequency-presetting signal C [6:0] is 1MHz; the phase noise is -85dBc/Hz at 10kHz offset.

Figure 11.7.5 shows the typical frequency-hopping characteristic of the synthesizer with frequency presetting. We started the synthesizer and changed the divider ratio N to make the frequency hop from 618 to 648MHz at 1000μs. The output signal V_a of the loop filter shows no change caused by the frequency hop, which means that the synthesizer is locked in immediately after the divider ratio N changes. The measured results indicate that the settling time is less than 10μs within the range of oscillation frequency of the synthesizer. Figure 11.7.6 shows the frequency-hopping characteristics of the synthesizer without the frequency-presetting function. The settling time is longer than 250μs, which is much longer than the synthesizer with frequency presetting.

The synthesizer includes compensation for variation in the oscillation frequency with the chip temperature as noted earlier. The temperature sensor and compensation circuit in the presetting module kept the VCO frequency stable as the temperature varied from -20 to 80°C.

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[1] J. Lee and B. Kim, "A Low Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1137-1145, Aug., 2000.
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[3] Tom A. D. Riley, Miles A. Copeland and Tad A. Kwasniewski, "Delta-Sigma Modulation in Fractional-N Frequency Synthesis," *IEEE J. Solid-State Circuits*, vol. 28, pp. 553-559, May, 1993.
[4] A. M. Fahim and M. I. Elmasry, "A Wideband Sigma-Delta Phase-Locked-Loop Modulator for Wireless Applications," *T. Circuits and Systems II*, vol. 50, pp. 53-62, Feb., 2003.

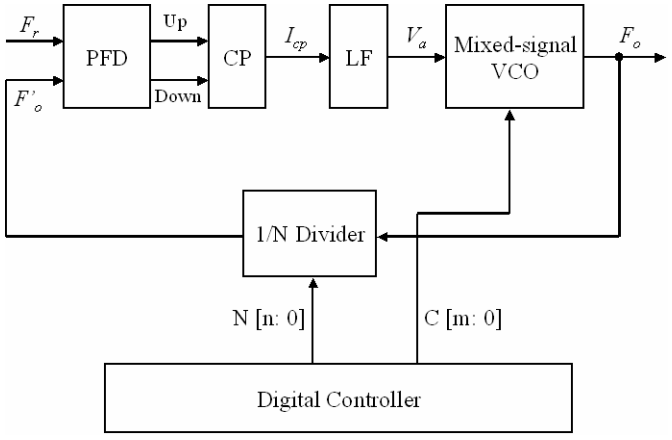

Figure 11.7.1: PLL frequency synthesizer with direct frequency presetting.

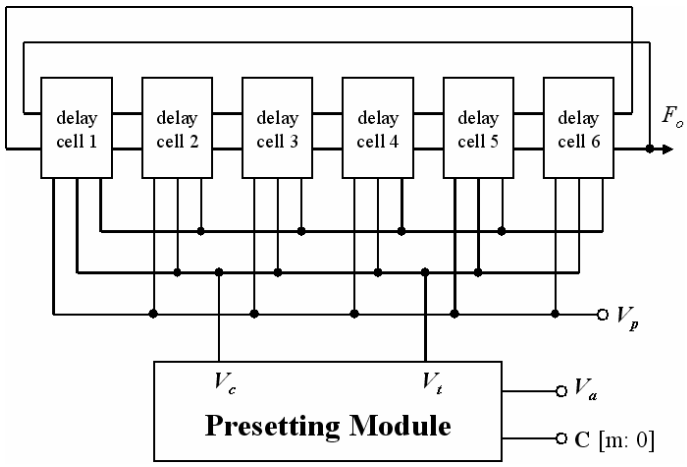

Figure 11.7.2: Mixed-signal VCO with presetting module.

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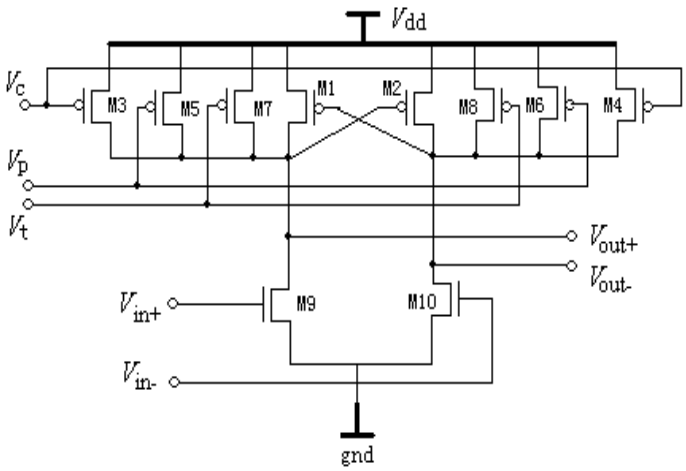

Figure 11.7.3: Delay cell in the VCO.

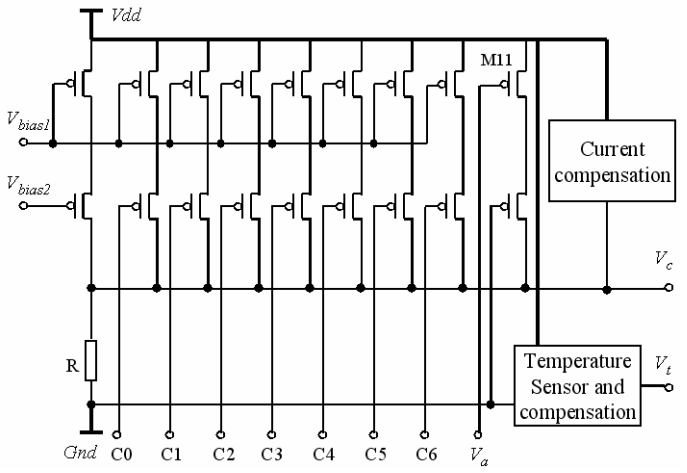

Figure 11.7.4: Mixed-signal presetting module.

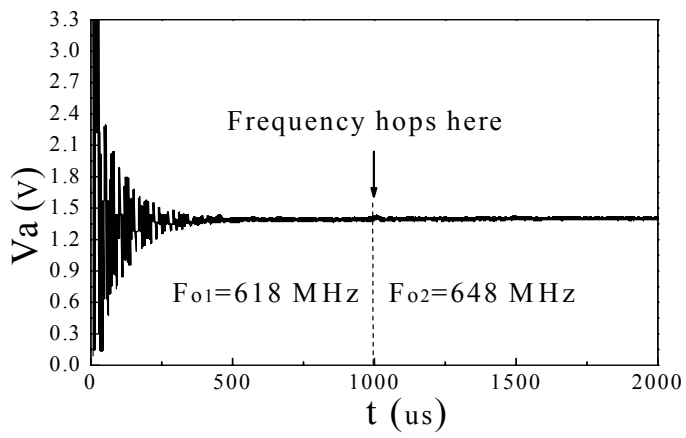

Figure 11.7.5: Frequency hopping characteristic WITH frequency presetting.

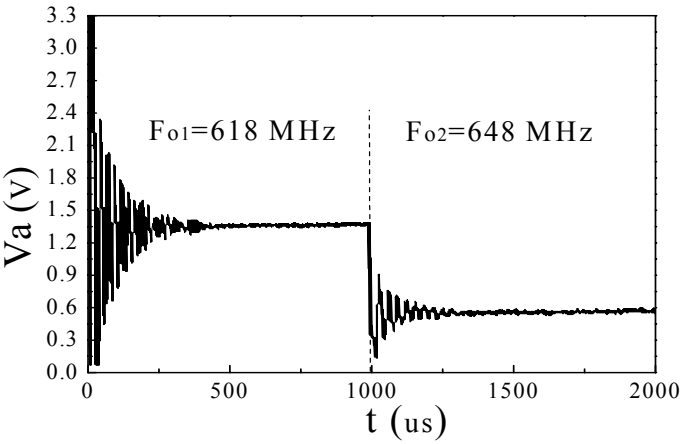

Figure 11.7.6: Frequency hopping characteristic WITHOUT frequency presetting.

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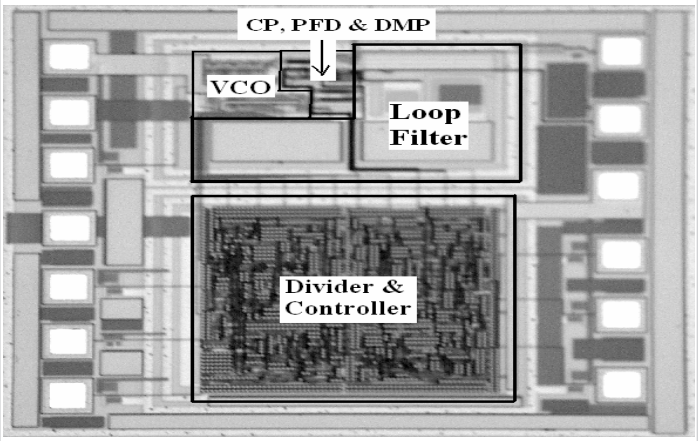

Figure 11.7.7: Chip micrograph.

